UniSLIC14 and the IDT821054/64 Programmable Quad CODEC

Application Note | May 2002 | AN9999.0

Author: Don LaFontaine

Reference Design using the UniSLIC14 and the IDT821054/64 Programmable Quad CODEC

The purpose of this application note is to provide a reference design for the UniSLIC14 and IDT821054/64 Programmable Quad CODEC.

The network requirements of many countries require the analog subscriber line circuit (SLIC) to terminate the subscriber line with an impedance for voiceband frequencies which is complex, rather than resistive (e.g. 600Ω). The UniSLIC14 accomplishes this impedance matching with a single network connected to the Z_T pin.

The IDT821054/64 Quad PCM CODEC uses an intergrated programmable DSP to realize AC Impedance Matching, Transhybrid Balance, Frequency Response Correction and Gain Setting functions.

Discussed in this application note are the following:

- 2-wire impedance matching.
- Receive gain (4-wire to 2-wire) and transmit gain (2-wire to 4-wire) calculations.
- Reference design for both 600Ω and 200Ω +680Ω||0.1µF (China Complex Impedance).

Impedance Matching

Impedance matching of the UniSLIC14 to the subscriber load is important for optimization of 2 wire return loss, which in turn cuts down on echoes in the end to end voice communication path. It is also important for maintaining voice signal levels on long loops. Impedance matching of the UniSLIC14 is accomplished by making the SLIC's impedance (Z_O, Figure 1) equal to the desired terminating impedance Z_L, minus the value of the protection resistors (R_P). The formula to calculate the proper Z_T for matching the 2-wire impedance is shown in Equation 1.

With the UniSLIC14 programmed to match a ZL of 600Ω, the IDT821054/64 uses an intergrated programmable DSP to realize any AC impedance.

$$Z_T = 200 \bullet (Z_{TR} - 2R_P) \quad \text{(EQ. 1)}$$

The value of Z_T with 30Ω protection resistors is108kΩ. The closest standard value is 107kΩ.

SLIC in the Active Mode

Figure 2 shows a simplified AC transmission model of the UniSLIC14 and the connection of the IDT821054/64 to the SLIC. Circuit analysis of the UniSLIC14 yields the following design equations:

$$V_A = I_M \times 2R_S \times \frac{1}{80k} \times 200(Z_{TR} - 2R_P) \times 5 \quad \text{(EQ. 2)}$$

$$V_A = \frac{I_M}{2}(Z_{TR} - 2R_P) \quad \text{(EQ. 3)}$$

Node Equation at UniSLIC14 V_{RX} input

$$\frac{V_{RX}}{500k} - \frac{V_A}{500k} = I_X \quad \text{(EQ. 4)}$$

Substitute Equation 3 into Equation 4

$$I_X = \frac{V_{RX}}{500k} - \frac{I_M(Z_{TR} - 2R_P)}{1000k} \quad \text{(EQ. 5)}$$

Loop Equation at UniSLIC14 feed amplifier and load

$$I_X 500k - V_{TR} + I_X 500k = 0 \quad \text{(EQ. 6)}$$

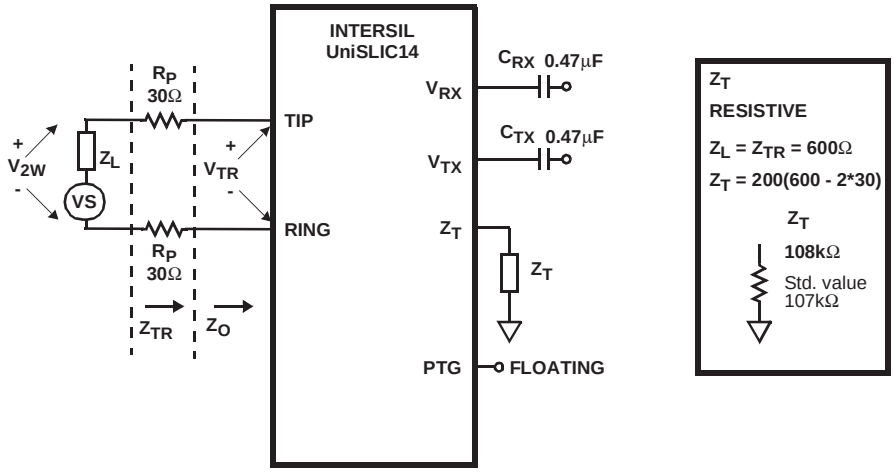

FIGURE 1. IMPEDANCE MATCHING

Substitute Equation 5 into Equation 6

$$V_{TR} = 2V_{RX} - I_M(Z_{TR} - 2R_P) \quad \text{(EQ. 7)}$$

Loop Equation at Tip/Ring interface

$$V_{2W} - I_M 2R_P + V_{TR} = 0 \quad \text{(EQ. 8)}$$

Substitute Equation 7 into Equation 8

$$V_{2W} = I_M Z_{TR} - 2V_{RX} \quad \text{(EQ. 9)}$$

Substituting $-V_{2W}/Z_L$ into Equation 9 for I_M and rearranging to solve for V_{2W} results in Equation 10.

$$V_{2W}\left(1 + \frac{Z_{TR}}{Z_L}\right) = -2V_{RX} \quad \text{(EQ. 10)}$$

where:

V_{RX} = The input voltage at the V_{RX} pin.

V_A = An internal node voltage that is a function of the loop current detector and the impedance matching networks.

I_X = Internal current in the SLIC that is the difference between the input receive current and the feedback current.

I_M = The AC metallic current.

R_P = A protection resistor (typical 30Ω).

Z_T = An external resistor/network for matching the line impedance.

V_{TR} = The tip to ring voltage at the output pins of the SLIC.

V_{2W} = The tip to ring voltage including the voltage across the protection resistors.

Z_L = The line impedance.

Z_O = The source impedance of the SLIC .

Z_{TR} = The input impedance of the SLIC including protection resistors.

Receive Gain (V_{RX} to V_{2W})

4-wire to 2-wire gain across the UniSLIC14 is equal to the V_{2W} divided by the input voltage V_{RX}, reference Figure 2.The receive gain is calculated using Equation 10.

Equation 11 expresses the receive gain (V_{RX} to V_{2W}) in terms of network impedances. From Equation 1, the value of Z_T was set to match the line impedance (Z_L) to the UniSLIC14 plus the protection resistors ($Z_O + 2R_P$). This results in a 4-wire to 2-wire gain of -1, as shown in Equation 11.

$$G_{4-2} = \frac{V_{2W}}{V_{RX}} = -2\frac{Z_L}{Z_L + Z_O + 2_{RP}} = -2\frac{Z_L}{Z_L + Z_L} = -1 \quad \text{(EQ. 11)}$$

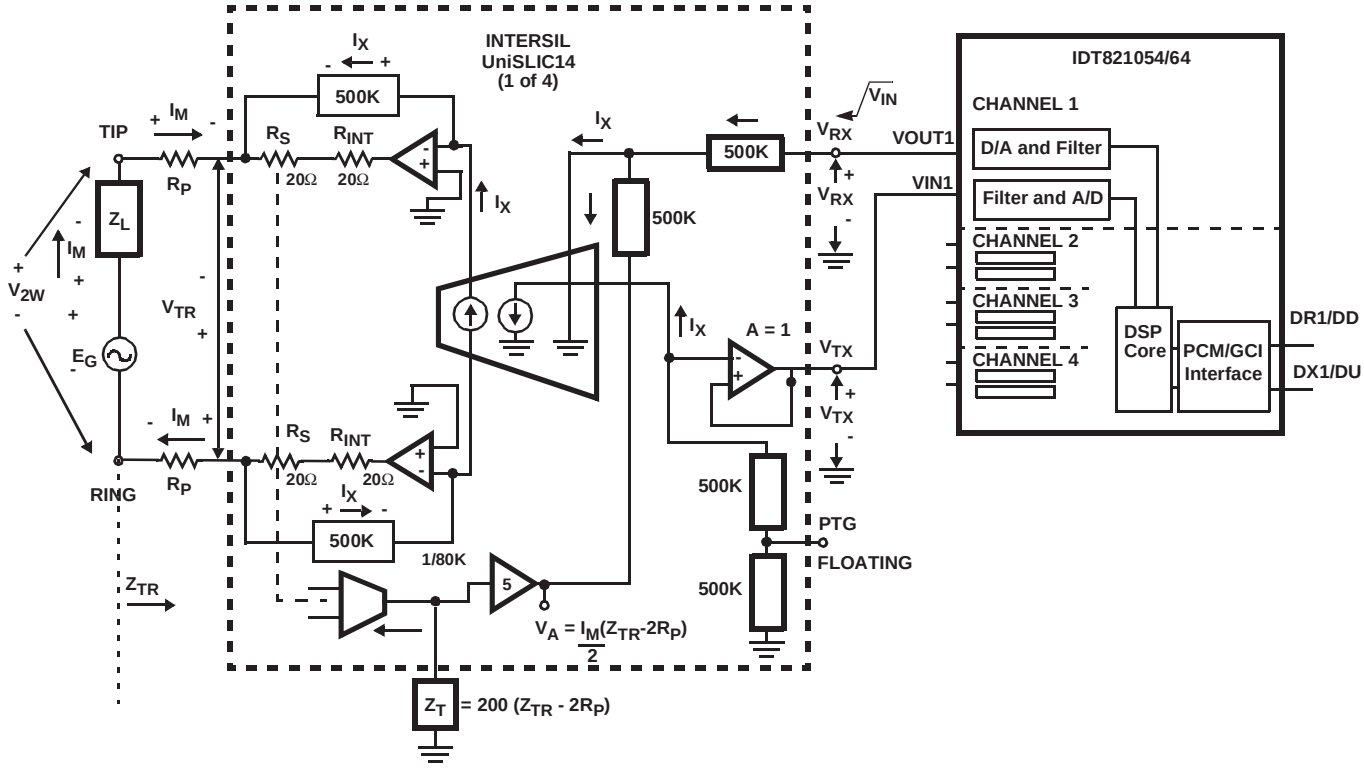

FIGURE 2. UniSLIC14 SIMPLIFIED AC TRANSMISSION CIRCUIT AND IDT821054/64

Receive Gain Across the System

The receive gain across the system is defined as the gain from the PCM highway to the phone (V_{2W}). With the receive gain through the UniSLIC14 set to 1, the receive gain across the system is entirely controlled by programming the IDT821054/64. The IDT821054/64 can program the receive gain across the system in two ways (reference Figure 3).

- The first is by programming the signal gain in its analog form. The analog receive gain, also known as Digital to Analog (D/A) gain, can be programmed in the IDT821054/64 to be either 0dB or -6dB.
- The second is by programming the signal gain (via. coefficients) when its in digital form. The digital form of the receive path can be programmed from +3 to -12dB with minimum 0.1dB steps.

This results in a possible receive gain (D/A) programming range from +3dB to -18dB. ***Note: Analog gain brings less noise than digital gain. When allocating the CODEC gain, the majority of the required gain should be preformed in the analog stage.***

Reference section titled “Information Required for IDT to Calculate IDT821054/64 CODEC DSP Coefficients” for information on obtaining coefficients for your design.

Transmit Gain Across UniSLIC14 (E_G to V_{TX})

The 2-wire to 4-wire gain is equal to V_{TX}/E_G with $V_{RX} = 0$, reference Figure 2.

Loop Equation

$$-E_G + Z_L I_M + 2R_P I_M - V_{TR} = 0 \quad \text{(EQ. 12)}$$

From Equation 7 with $V_{RX} = 0$

$$V_{TR} = -I_M(Z_{TR} - 2R_P) \quad \text{(EQ. 13)}$$

Substituting Equation 13 into Equation 12 and simplifying.

$$E_G = I_M(Z_L + Z_{TR}) \quad \text{(EQ. 14)}$$

By design, $V_{TX} = -V_{TR}$, therefore,

$$G_{2\text{-}4} = \frac{V_{TX}}{E_G} = \frac{I_M(Z_{TR} - 2R_P)}{I_M(Z_L + Z_{TR})} = \frac{(Z_{TR} - 2R_P)}{(Z_L + Z_{TR})} \quad \text{(EQ. 15)}$$

A more useful form of the equation is rewritten in terms of V_{TX}/V_{2W}. A voltage divider equation is written to convert from E_G to V_{2W} as shown in Equation 16.

$$V_{2W} = \left(\frac{Z_{TR}}{Z_{TR} + Z_L}\right) E_G \quad \text{(EQ. 16)}$$

Rearranging Equation 16 in terms of E_G, and substituting into Equation 15 results in an equation for 2-wire to 4-wire gain that’s a function of the synthesized input impedance of the SLIC and the protection resistors (Z_{TR}).

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{2W}} = \frac{Z_{TR} - 2R_P}{Z_{TR}} = \frac{600 - 60}{600} = 0.9 \quad \text{(EQ. 17)}$$

To match a 600Ω line, Z_{TR} is set to 595Ω (EQ 1, 107k/200+60) where R_P is equal to 30.0Ω. This results in a 2-wire to 4-wire gain of 0.9 or -0.915dB (EQ 17, 595-60/595).

Notice that the phase of the 2-wire to 4-wire signal is in phase with the input signal and that the gain will always be less than one because of the protection resistors.

Transmit Gain Across the System

The transmit gain across the system is defined as the gain from the phone or 2-wire side (V_{2W}) to the PCM highway. Setting the gain of the IDT821054/64 will have to account for the attenuated signal through the UniSLIC14. The system gain is entirely controlled by programming the IDT821054/64. The IDT821054/64 can program the transmit gain across the system in two ways (reference Figure 3).

- The first is by programming the signal gain in its analog form. The analog transmit gain, also known as Analog to Digital (A/D) gain, can be programmed in the IDT821054/64 to be either 0dB or +6dB.
- The second is by programming the signal gain (via. coefficients) when its in digital form. The digital form of the transmit path can be programmed from -3dB to +12dB with minimum 0.1dB steps.

This results in a possible transmit gain (A/D) programming range from -3dB to +18dB. ***Note: Analog gain brings less noise than digital gain. When allocating the CODEC gain, the majority of the required gain should be preformed in the analog stage.***

Reference section titled “Information Required for IDT to Calculate IDT821054/64 CODEC DSP Coefficients” for information on obtaining coefficients for your design.

Transhybrid Balance G(4-4)

Transhybrid balance is a measure of how well the input signal is canceled (that being received by the SLIC) from the transmit signal (that being transmitted from the SLIC to the CODEC). Without this function, voice communication would be difficult because of the echo. The Transhybrid balancing filter inside the IDT821054/64 is used to adjust transhybrid balance to ensure the echo cancellation meets the ITU-T specifications. The coefficient for Echo Cancellation is ECF.

Frequency Response Correction

The FRR filter in the receive path and the FRX filter in the transmit path can be programmed to correct any frequency distortion caused by the impedance matching filters. The coefficients of Frequency Response Correction are FRR for receive path and FRX for the transmit path.

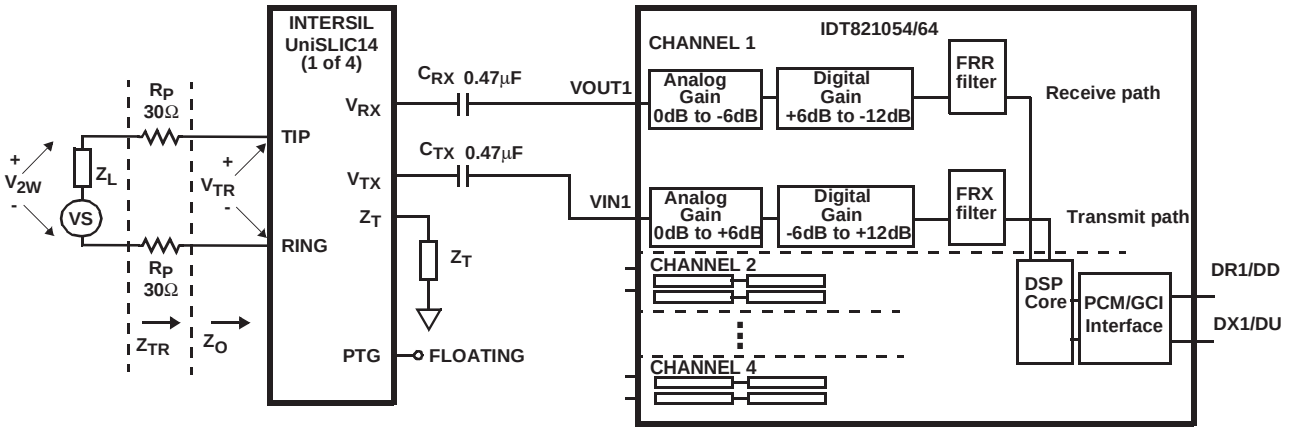

FIGURE 3. RECEIVE GAIN G(4-2), TRANSMIT GAIN (2-4)

Information Required for IDT to Calculate IDT821054/64 CODEC DSP Coefficients

For IDT to calculate IDT821054/64 DSP coefficient, customers should provide the following information about their subscriber line card:

- Accurate SLIC PSPICE model. It can be provided in .lib file or PSPICE schematic file.
- System Impedance
- Gain (Transmit path and Receive path)

Using the DSP coefficients provided by IDT, the overall performance of the system will pass ITU-T requirements.

When the COF RAM button is selected from the MPI Operation General Interface screen, the COF RAM Operation screen will appear (Figure 4). From this screen, the user can configure all the coefficients for the current channel.

FIGURE 4. COEFFICIENT RAM OPERATION SCREEN

Reference Design of the UniSLIC14 and the IDT821054/64 With a 600Ω Load

The design criteria is as follows:

- 4-wire to 2-wire gain (DR1/DD to V_{2W}) equal 0dB
- 2-wire to 4-wire gain (V_{2W} to DX1/DU) equal 0dB
- Rp = 30Ω

Figure 5 gives the reference design using the Intersil UniSLIC14 and the IDT821054/64 Programmable Quad PCM CODEC. Also shown in Figure 5 are the voltage levels at specific points in the circuit.

Impedance Matching

The 2-wire impedance is matched to the line impedance Z_0 using Equation 1, repeated here in Equation 18.

$$Z_T = 200 \bullet (Z_{TR} - 2R_P) \quad \text{(EQ. 18)}$$

For a line impedance of 600Ω, Z_T equals:

$$Z_T = 200 \bullet (600 - 60) = 108k\Omega \quad \text{(EQ. 19)}$$

The closest standard value for Z_T is 107kΩ.

However, it would be very convenient and cost effective if system manufacturers can use only one type of line card to meet different impedance requirements and different gain requirements. The programmability of IDT821054/64 can help system manufactures to reach this goal. By using different coefficients this reference design can meet both 600Ω and $200\Omega + 680\Omega||0.1\mu$ F impedance requirements.

With the value of Z_T selected to be $107k\Omega \pm 1\%$, the coefficients for Transmit Gain (A/D) and Receive Gain of zero (with a line impedance of 600Ω) is given in Table 1.

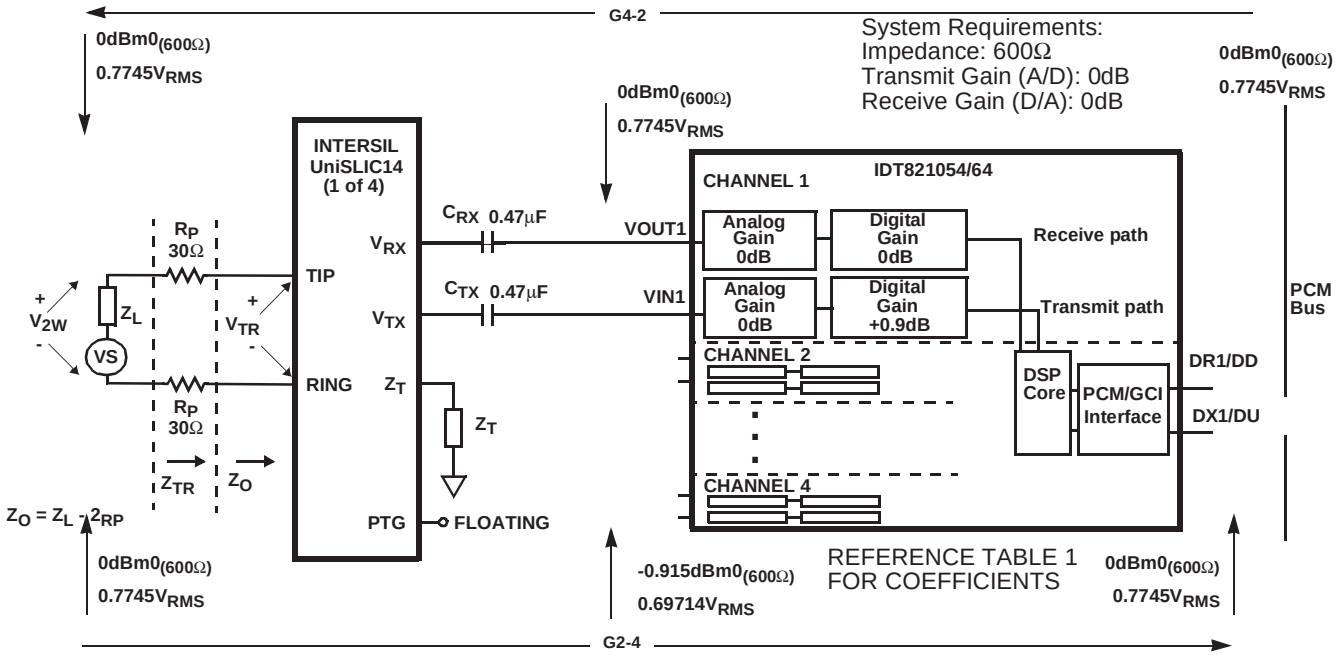

FIGURE 5. REFERENCE DESIGN OF THE UniSLIC14 AND THE IDT821054/64 WITH A 600Ω LOAD IMPEDANCE

Specific Implementation for China

The design criteria for a China specific solution are as follows:

- Desired line circuit impedance is 200 + 680//0.1μF
- Receive gain (V_{2W}/(DR1/DD)) is -3.5dB
- Transmit gain ((DX1/DU)/V_{2W}) is 0dB
- 0dBm0 is defined as 1mW into the complex impedance at 1020Hz
- R_p = 30Ω

Figure 6 gives the reference design using the Intersil UniSLIC14 and the IDT821054/64 Programmable Quad CODEC. Also shown in Figure 6 are the voltage levels at specific points in the circuit. These voltages will be used to adjust the gains of the network.

Adjustment to Get -3.5dBm0 at the Load Referenced to 600Ω

The voltage equivalent to 0dBm0 into 811Ω ($0dBm0_{(811Ω)}$) is calculated using Equation 20 (811Ω is the impedance of complex China load at 1020Hz).

$$0dBm_{(811\Omega)} = 10\log\frac{V^2}{811(0.001)} = 0.90055V_{RMS} \quad \text{(EQ. 20)}$$

The gain referenced back to $0dBm0_{(600\Omega)}$ is equal to:

$$GAIN = 20\log\frac{0.90055V_{RMS}}{0.7745V_{RMS}} = 1.309dB \quad \text{(EQ. 21)}$$

The adjustment to get -3.5dBm0 at the load referenced to 600Ω is:

$$Adjustment = -3.5dBm0 + 1.309dBm0 = -2.19dB \quad \text{(EQ. 22)}$$

The voltage at the load (referenced to 600Ω) is given in Equation23:

$$-2.19dBm_{(600\Omega)} = 10\log\frac{V^2}{600(0.001)} = 0.60196V_{RMS} \quad \text{(EQ. 23)}$$

Impedance Matching

Contact IDT for specific coefficiens for this design.

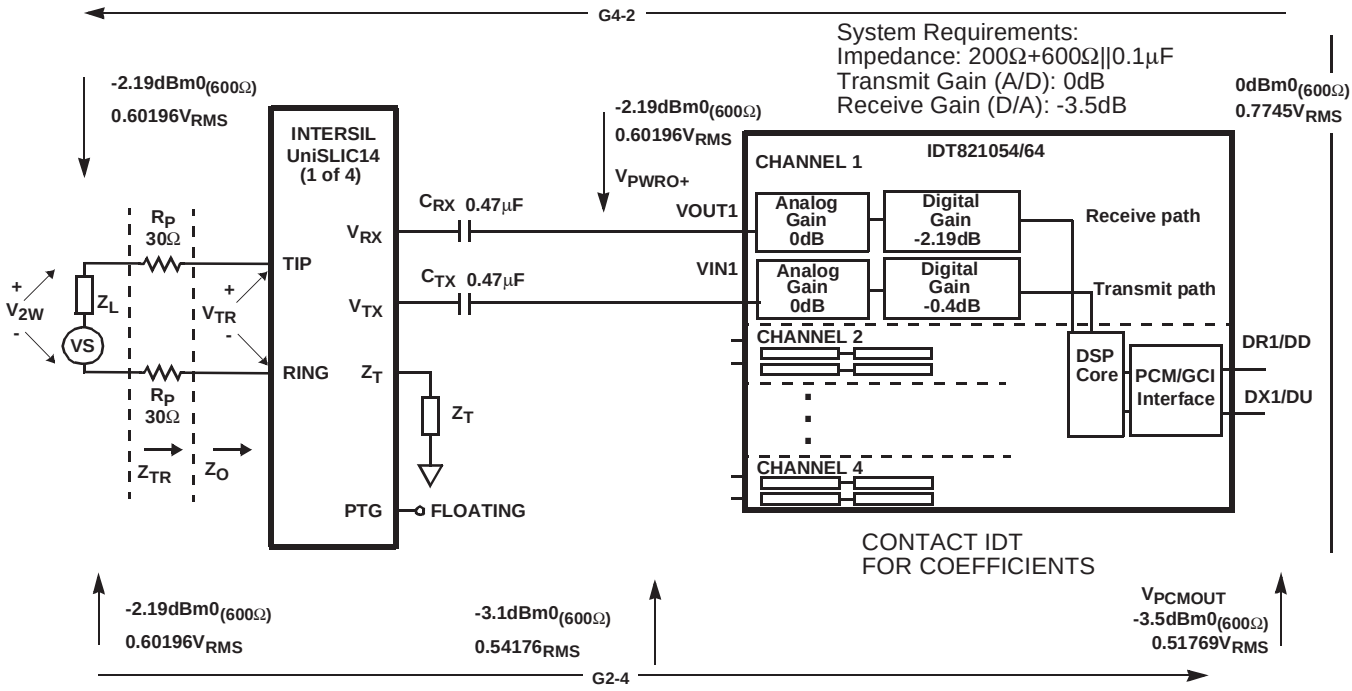

FIGURE 6. REFERENCE DESIGN OF THE UniSLIC14 AND THE IDT821054/64 WITH CHINA COMPLEX LOAD IMPEDANCE

TABLE 1. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB)

Coefficient RAM				**CHANNEL 1**													
IMF:	04	00	EE	FF	00	00	00	00	00	00	00	00	00	00	00	00	
ECF:	C2	08	00	00	00	00	00	0	00	00	A2	5E	75	D9	00	00	
KM:	00	00	00	02	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	D7	00	F9	EF	16	25	16	25	F9	EF	D7	00	99	31	***GTX***	FF	1F
ACR:	FF	00	84	FE	49	3F	49	3F	84	FE	FF	00	CE	84	***GRX***	0C	03
Coefficient RAM				**CHANNEL 2**													
IMF:	04	00	EE	FF	00	00	00	00	00	00	00	00	00	00	00	00	
ECF:	C2	08	00	00	00	00	00	0	00	00	A2	5E	75	D9	00	00	
KM:	00	00	00	02	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	D7	00	F9	EF	16	25	16	25	F9	EF	D7	00	99	31	***GTX***	FF	1F
ACR:	FF	00	84	FE	49	3F	49	3F	84	FE	FF	00	CE	84	***GRX***	0C	03
Coefficient RAM				**CHANNEL 3**													
IMF:	04	00	EE	FF	00	00	00	00	00	00	00	00	00	00	00	00	
ECF:	C2	08	00	00	00	00	00	0	00	00	A2	5E	75	D9	00	00	
KM:	00	00	00	02	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	D7	00	F9	EF	16	25	16	25	F9	EF	D7	00	99	31	***GTX***	FF	1F
ACR:	FF	00	84	FE	49	3F	49	3F	84	FE	FF	00	CE	84	***GRX***	0C	03

TABLE 1. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB) (Continued)

Coefficient RAM				CHANNEL 4													
IMF:	04	00	EE	FF	00	00	00	00	00	00	00	00	00	00	00	00	
ECF:	C2	08	00	00	00	00	00	0	00	00	A2	5E	75	D9	00	00	
KM:	00	00	00	02	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	D7	00	F9	EF	16	25	16	25	F9	EF	D7	00	99	31	***GTX***	FF	1F
ACR:	FF	00	84	FE	49	3F	49	3F	84	FE	FF	00	CE	84	***GRX***	0C	03